# Digital Signal Processing—Up to Microwave Frequencies

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*Invited Paper*

***Abstract*—Digital logic integrated circuits are advancing toward ever higher speeds of operation. Clock frequencies already exceed 1 GHz in some Si CMOS-based consumer products, and even higher speeds are attainable in specialized technologies, such as those based on GaAs, InP, and SiGe bipolar and field-effect transistors. Digital approaches may be used to carry out a variety of functions important in microwave systems, including signal generation, filtering, and frequency conversion. The digital implementation provides a variety of potential benefits, including lack of sensitivity to aging and component inaccuracies, flexibility, and programmability. The dynamic range and degree of nonlinearity can be specified by design. Signal storage and memory functions are easily accomplished. Single-chip integration of digital and microwave systems are also facilitated. The application of digital techniques in domains previously considered to be analog is an important ongoing technology thrust, which may be expected to accelerate. Critical interfaces between the digital and analog domains are provided by analog-to-digital converters, digital-to-analog converters, and fractional-$N$ frequency synthesizers. This paper reviews the prospects of digital techniques for microwave systems, and briefly describes the state-of-technology and future possibilities.**

***Index Terms*—Analog-to-digital conversion, digital signal processing, digital-to-analog conversion, high-speed digital integrated circuits.**

## I. Introduction

SIGNAL processing (including amplification, filtering, frequency generation, frequency conversion, and modulation) at microwave frequencies has traditionally been carried out with analog circuits. However, digital circuits are steadily advancing in capabilities. The technology advances promise to allow digital techniques to be used at frequencies well into the microwave region.

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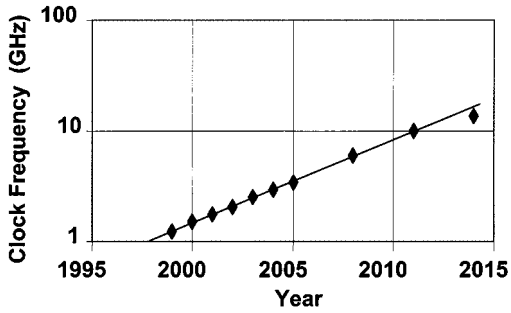


Fig. 1. Progression of clock rate for high-performance CMOS logic ICs according to the ITRS Roadmap.

Digital signal processing (DSP) is already widely used in signal processing at baseband frequencies, for example, for audio and video signals. In wireless communications, DSP use has grown very rapidly, and is now a mainstay of most mobile communication systems. The interface between digital and analog sometimes is at baseband frequencies, and increasingly at IF frequencies.

The advance of digital CMOS circuits is embodied approximately in Moore's law (according to which the computational capability of digital CMOS chips doubles every 18 months). A detailed projection of expected integrated circuit (IC) characteristics is contained in the ITRS Roadmap [1]. Fig. 1 illustrates the trend in clock rate for high-end application specific large CMOS-based logic circuits. Clock rates surpassing 3.5 GHz are expected in the next several years (corresponding to scaled gate-lengths on the order of 0.1 $\mu$m), and they will reach 10 GHz by 2012. There is a corresponding trend in the improvement of general-purpose DSP chips. Fig. 2 illustrates the decrease in power needed for signal processing [2] (expressed in millions of instructions per second).

With IC technologies optimized for high speed, the generation and processing of digital signals for optical fiber transmission has reached 10 Gbs in fielded systems, and 40 Gbs (or above) in the laboratory. The digital signals have spectral densities that extend essentially from dc to a frequency of 3/4 of the bit rate. The circuitry under development for these applications is an area of great excitement.

The availability of high-speed DSP techniques opens up potentially revolutionary new possibilities in microwave system design. The introduction of complex digital circuits with clock rates well into the microwave region (and bordering the

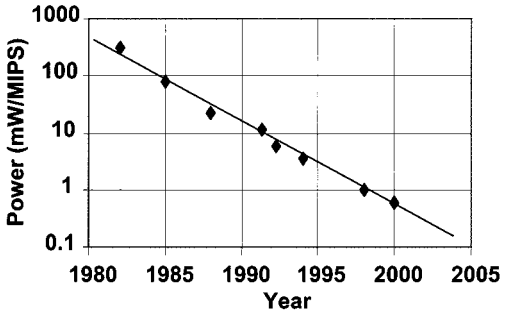


Fig. 2. Trend of power dissipation needed to accomplish DSP operations versus time for general-purpose DSP chips.

millimeter-wave region) is potentially paradigm shifting. This paper summarizes present applications of DSP in microwave systems, illustrates the new opportunities, and discusses the trends in technology that may allow this potential to be realized. The focus of the paper is on applications in classical narrow-band microwave systems rather than on broad-band systems such as those for optical fiber transmission.

## II. Characteristics of DSP

The use of digital, rather than analog, techniques for signal processing provides a variety of potential advantages. These include the following:

1) absence of tuning requirements of conventional microwave circuits, and inherent reproducibility of characteristics;
2) independence from aging, temperature effects, and mismatches due to fabrication tolerances;
3) control over the signal-to-noise ratio and the distortion introduced by the system, which can be traded off, by design, for circuit complexity;
4) immunity to interference from low-level noise sources, crosstalk, and power supply variations;
5) ability to provide unique functions, such as signal storage, amplification with a specified degree of nonlinearity, encryption, and error correction;
6) reconfigurability and programmability, such that potentially fixed hardware could be used with software control to implement a wide variety of functions, or to address a variety of air-interface standards;
7) simplified testing, possibly with system self-test;
8) possibility of integration of both microwave and digital portions of the system in a single chip ("system-on-a-chip").

Digital processing has a variety of unique features, which are sometimes challenging to deal with. The conversion of signals from the analog to the digital domain is unavoidably accompanied by the introduction of noise ("quantization noise"), related to the number of bits used in the conversion (resolution). Introduction of thermal noise during the conversion is also a concern. The analog-to-digital conversion process also is highly nonlinear, thus, it can introduce "noise" associated with frequencies outside of the Nyquist band that get folded into the signal band during the conversion process; it can also cause harmonic generation and intermodulation associated with the signal even if the signal is band-limited.

According to the Nyquist sampling theorem, to represent a signal of bandwidth $B$, a sample rate $fs$ of at least $fs = 2B$ is required. Assuming equally spaced quantization steps with voltage step size $\Delta$, the quantization noise can often be modeled as having overall variance $V_n^2$ given by $V_n^2 = \Delta^2/12$. For highly time-varying aperiodic signals and high resolution, the noise often appears as "white" noise with constant power spectral density over the Nyquist band. The dynamic range $D$ of the output (the ratio of the full-scale signal power to the in-band noise power for sinusoidal signals that are represented digitally) is typically given by $D = 3/2^*2^{2m}$, or in decibels, $D\,(\text{dB}) = 6.02m + 1.8$, where $m$ is the number of bits used in the converter. For radio receivers, for example, a dynamic range near 85 dB is often desired; this corresponds to 14 bits of resolution.

With low-resolution quantization or with periodic input signals, the extra "noise" power introduced by quantization has the form of discrete spurious signals. Since these extra frequencies are often undesirable in systems, they can be reduced by adding "dither" to the input signal, spreading the noise power over a wide spectral band (but also adding noise).

In order to carry out signal-processing operations based on additions and multiplications, word widths at least as large as the resolution $m$ must be used. Truncation of wider words obtained after operations adds additional noise that must be considered in detail for a given application.

In order to carry out the required digital-processing operations, substantial power may be required. The dc power associated with digital processing depends on the IC technology adopted. For the case of CMOS, basic switching of logic gates requires the expenditure of energy $E = (1/2)CV_d^2$ per clock cycle (where $V_d$ is the power supply voltage and $C$ is the load capacitance). For a given processing function, the power dissipated in the DSP is then given by

$$P_{\text{digital}} = \alpha C V_d^2 f_{\text{clk}} m^c \tag{1}$$

where $\alpha$ denotes the fraction of gates whose outputs switch, and $c$ is a coefficient that depends on the operations performed and algorithms used ($c = 1$ for addition or scaling; $c \sim 2$ for multiplication, etc.). As technology progresses, $C$ and $V_d$ tend to decrease, predominantly due to dimensional scaling. The ability to scale down $C$ on-chip (and, correspondingly, to employ high load impedance levels on-chip while achieving high speed) is a key strength of the digital approach. Gate input capacitances down to 1 fF are achieved with the most advanced circuits.

By contrast, with analog signal processing, it is typical to work with impedance levels much closer to 50 $\Omega$, and the power dissipation per operation (such as amplification or filtering) is typically much larger. In an optimized amplifier or filter, the required power dissipation for analog operations with a given bandwidth $B$ and dynamic range $D$ is typically given by

$$P_{\text{analog}} = \text{const}\, KTBFD \tag{2}$$

where $K$ and $T$ are Boltzmann's constant and the absolute temperature, and $F$ is the noise figure of the amplifier [3].

It is interesting to note that (1) and (2) are related. To provide proper frequency response in the digital system, the Nyquist sampling theorem dictates $f_{\rm clk} > 2B$ (or, more generally, $f_{\rm clk} = 2B^*{\rm OSR}$, where "OSR" denotes the oversampling ratio). The noise associated with charging the capacitance $C$ through a noisy resistor leads to noise voltage with standard deviation $V_n = [KT/C]^{1/2}$. The requirements of error-free digital computation dictate that $V_n \ll V_d$ (at present, $V_d > 500V_n$, but in the future, $V_d = 15V_n$ could be employed in scaled devices while still achieving low enough error rate). Then

$$P_{\rm digital} = \alpha KTB\,{\rm OSR}\left(\frac{V_d}{V_n}\right)^2 m^c. \tag{3}$$

$P_{\rm digital}$ tends to be larger than $P_{\rm analog}$ due to the factors $(V_d/V_n)^2$ and OSR. It is important to note, however, that $P_{\rm digital}$ increases with dynamic range $D$ as $m^c = [\log_2(D)]^c$, while for analog processing, it is typical to find $P$ proportional to $D$, as noted in (2). This result illustrates that the conversion from analog to digital techniques compares best in terms of power dissipation in the regime of very high dynamic range.

## III. IC Technologies for Very High-Speed Digital Circuits

Numerous high-speed digital technologies have been developed, including Si CMOS; bipolar technologies based on Si, SiGe, GaAs and InP; and FET-based technologies employing GaAs and InP. The technologies differ in attainable clock speed (which is closely related to the current-gain cutoff frequency $f_t$), as well as integration level and power dissipation. The speed of all technologies depends to a great extent on the transit time of carriers across the device $T_{\rm tr}$ (typically $f_t = 1/2\pi T_{\rm tr}$). As technology has progressed, the device dimensions have been scaled down, and the values of $T_{\rm tr}$ have decreased. At the same time, the voltages used in the system have been perforce scaled down to avoid breakdown; happily, lower voltage reduces power dissipation (although it is increasingly difficult to translate the logic voltage levels to large-signal swings at the system output, for example, in a power amplifier).

The speed capability of digital technologies has been often gauged by the maximum operating speed of frequency dividers. As well as being demonstration vehicles, these circuits are used directly in phase-locked loops, as detailed below. The frequency dividers most representative of conventional logic are static dividers, operable down to essentially dc. Higher speed results can be obtained from dynamic dividers, which do not operate properly at low speed. Table I summarizes a variety of recently reported operating speeds of frequency dividers implemented in different technologies [4]–[15].

All logic families dissipate static power (i.e., even if not actively switching), except CMOS. The static power dissipation is not a great concern in circuits that are active virtually all the time (such as frequency dividers and circuits for optical fiber communications, etc.), but is progressively more burdensome in larger circuits, in which only a small fraction of the gates switch during a given cycle.

Si CMOS is the dominant digital technology in commercial production. It can attain levels of integration in the hundreds of millions of transistors per chip, far surpassing other technologies. Production chips employ gate lengths down to 0.13 $\mu$m and, as described in the ITRS Roadmap, the gatelength will further shrink to below 0.05 $\mu$m (these devices have already been demonstrated on a laboratory basis) [16]. $F_t$ values for nFET above 140 GHz, and for pFETs above 110 GHz have been reported although, for current production circuits, the corresponding values are of the order of 40 GHz. In the scaled devices, there are a variety of problems associated with leakage currents from source to drain and across the thin oxide gate insulators, although these are being addresses by research efforts worldwide [17].

TABLE I
Representative Frequency-Divider Performance for Various Digital IC Technologies

| Technology | Maximum Frequency | Circuit Type |
|---|---|---|
| **Si CMOS** | 26.5 GHz | Dynamic |
| | 16.8 GHz | Static |
| **Si bipolar** | 30 GHz | Static |
| **SiGe HBT** | 53GHz | Static |
| | 82GHz | Dynamic |
| **GaAs HBT** | 40GHz | Static |
| **GaAs HFET** | 51 GHz | Dynamic |
| **InP HBT** | 72.8 GHz | Static |
| | 80 GHz | Dynamic |
| **InP HFET** | 76GHz | Dynamic |
| | 74GHz | Dynamic |

Bipolar technology benefits from a vertical device structure (in contrast to the lateral structure of the FETs). In conventional Si bipolar devices, the thickness of the base (which controls $f_t$ in a manner roughly equivalent to FET gatelength), can be as low as 0.05 $\mu$m. The devices have high transconductance, excellent matching between transistor characteristics, and $f_t$ values that exceed 50 GHz. The technology can be improved by the use of SiGe in the base region of the device. This can provide a built-in field, which drives electrons by drift as well as diffusion, reducing base transit time. SiGe heterojunction bipolar transistors (HBTs) have been very actively developed in recent years. Recent production corresponds to $f_t$ values of 80 GHz, while reported laboratory demonstrations show values above 180 GHz. More generally, the combination of different materials within a given transistor (heterostructures) adds a powerful tool for optimizing device characteristics. It is also used in bipolar devices to improve the emitter injection efficiency and allow higher base doping (and lower base resistance) than attainable in conventional devices.

The use of III–V semiconductors allows shorter transit times and higher $f_t s$ as a result of improved electron transport characteristics (high mobility and high peak velocity), as

well as providing benefits of reduced device and interconnect capacitance from the use of semiinsulating substrates. The materials available to form heterostructures is much wider than for Si technology, enabling more dramatic improvement in characteristics. In the III–V bipolar area, GaAs/AlGaAs and GaAs/GaInP HBTs have received the most work, and are in widespread production for microwave circuits (such as power amplifiers). Recent fabrication lines have employed 6-in wafers. These HBTs have attained $f_t$ values as high as 170 GHz, and have been used in digital circuits with transistor counts up to 10 000. HBT technologies based on InP are currently under intense development because of their promise for even higher speeds. $F_t$ values up to 250 GHz have been reported for these devices. A novel fabrication scheme in which the HBT active layers are transferred from the substrate on which they are grown in order to carry out processing on both top and bottom sides of the active devices has yielded very high performance results, including maximum frequency of oscillation (which depends on high $f_t$, as well as on low parasitic capacitances and resistances) in excess of 1 THz [18].

FETs based on III–V materials have been developed for digital, as well as microwave applications. The n-channel FETs are inherently higher speed than corresponding Si FETs. P-channel FETs, however, tend to be lower speed than in Si and, as a result, complementary logic has not been used extensively. Logic families based on enhancement FET switches with depletion mode loads are frequently used. With ion-implanted GaAs, ICs with gate counts in the range of 1 million have been made. Higher speed results are achievable with heterostructure FETs, which benefit from modulation doping to improve carrier mobility, improve control over the channel design, and reduce gate current. With very short gate lengths, $f_t$ values in excess of 200 GHz have been obtained with heterostructures grown on GaAs substrates that employ AlGaAs barrier layers, and have channels of InGaAs, forming a pseudomorphic high electron-mobility transistor (pHEMT). Even higher values are attained in related structures grown on InP substrates, employing InAlAs barriers and InGaAs channels; $f_t$ as high as 350 GHz have been reported [19]. These record $f_t s$ are obtained in individual transistors. Digital IC technologies with $f_t$ of the order of 150 GHz have been developed.

Among the most significant applications of ultrahigh-speed digital circuits are the generation of signals for optical fiber transmission systems. The circuits developed for this application and the state-of-the-art have been the subject of a number of excellent reviews [20], [21]. Initial demonstrations have been made of multiplexers (or serializers) operating up to 80 Gb/s. These very broad-band systems have new challenges both in device design and fabrication, as well as in packaging (since the objective is generally to maintain flat response from dc (or perhaps 100 kHz) to 60 GHz.

## IV. Microwave/DSP Interfaces

A pacing element in the application of digital techniques in microwave systems is the availability of accurate high-bandwidth low-cost circuits for digital-to-analog (D/A) conversion and analog-to-digital conversion. The development of these circuits has been an ongoing research activity for many years.

### *A. Digital-to-Analog Converters (DACs)*

D/A conversion is most often carried out by combining the outputs of many individual current sources or charge generators, where the individual sources are switched on or off by the digital input bits. Ideally, current sources (for example) with binary weighting can be used, one for each input bit. Binary weighting can be done by construction (such as by changes in FET width, bias resistor value, etc.) or by means of current division from a source of standard value, in $R-2R$ or $C-2C$ ladders. In practice, it is difficult to maintain high accuracy over the different weighted sources of widely disparate values needed for high-resolution converters. One possible solution is to provide one current source of standard size for each of the $2^m-1$ input possibilities. This brute-force approach cannot be used for resolution above about 10 bits (requiring 1023 sources); hybrid approaches are often used, using a combination of ladders and paralleled unit sources.

Different high-speed IC technologies have different strengths for implementing subcircuits of interest in high-performance DACs. Matching of elements, as needed in fabricating current sources of equal value, is most easily accomplished with bipolar technologies. Transition speed in the switches is achieved by high $f_t$ transistors. It is desirable, however, to use FETs in the switches controlling the current sources for the different bits; by contrast, bipolar transistors consume base current (and so their collector current is not exactly equal to their emitter current), and they cannot be operated in saturation for high-speed applications. The availability of semiinsulating substrates is worthwhile for high-speed purposes.

Numerous techniques have emerged to overcome the inherent deficiencies of different technologies. To accomplish matching of current sources in a CMOS technology, the availability of large integration levels can be exploited by implementing on-chip calibration techniques; or by monitoring errors, storing their values in a lookup table, and correcting them with a special DAC; or by scrambling the unit current sources in successive output samples so that "on-average" the output only senses the mean values of the sources. Oversampling and delta–sigma techniques (addressed below for A/D converters) may also be employed. In this approach, low-resolution DACs are operated at speeds much higher than the Nyquist frequency. The overall DAC output, after filtering, can be highly accurate in the frequency band of interest. A particularly useful limiting case is to use a 1-bit DAC, which inherently has no mismatch problem at all, to implement high-resolution outputs.

Dynamic errors (that arise because of nonideal transients in the output of the switches and sources) are harder to cure. High $f_t$ transistors operated with high currents tend to minimize these problems. Accurate on-chip synchronization of the switching of the multiple sources is also required. Alternately, the output of the DAC can be provided with a sample-and-hold or other switching circuit to disconnect the DAC from the output during the time the on-chip subcircuits are settling. The output is then often in a return-to-zero format. This technique decorrelates the output settling from the past history of the signal.

DACs are characterized by resolution and maximum sampling rate, as well as by static linearity (differential and inte-

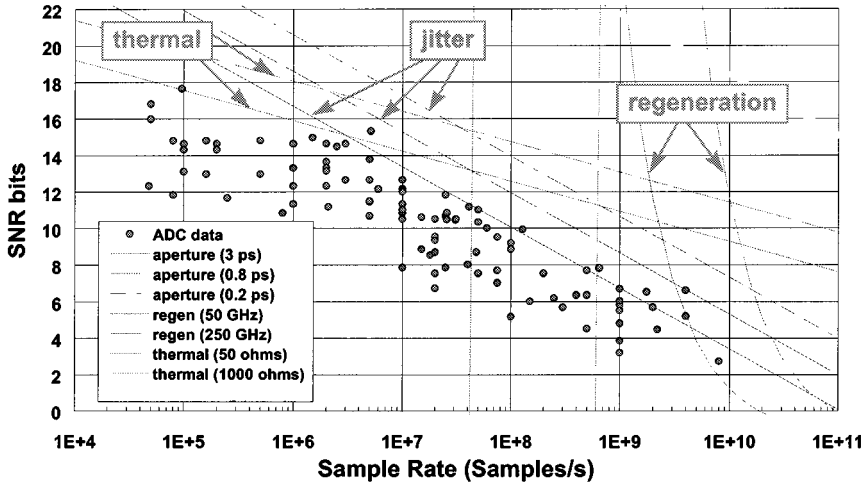


Fig. 3. Walden plot, showing stated resolution versus maximum sampling rate, for a variety of recently reported ADCs.

gral) and by dynamic effects. Particularly for microwave applications, typical test patterns correspond to the generation of a single sinusoid. Imperfect DACs have outputs showing spurious frequencies in addition to the desired tone. Test signals derived from direct digital frequency synthesizers (described in Section IV) are among the best test patterns available for high-performance DACs.

In the microwave region, DAC operation at 3 GS/s with 8-bit resolution has been demonstrated. In the context of a DDS system, this DAC permits generation of sinusoids with frequencies up to 1.5 GHz, with spurious-free dynamic range of the order of 50 dBc.

### *B. Analog-to-Digital Converters (ADCs)*

Comprehensive surveys of high-performance ADCs have recently been done [22], [23]. Fig. 3 presents a chart in which the maximum sampling rate and the nominal resolution of reported high-performance ADCs are plotted. This chart, widely known as the "Walden plot," illustrates the tradeoff between sampling rate and resolution, generally corresponding to a slope of 1 bit per octave of sampling rate. By tracking the limiting performance of ADCs in similar charts over a period of time, Walden has shown that ADC performance is advancing at a rate of approximately 1 bit per 6–8 years at a fixed sampling rate (or, conversely, $\times 2$ increase in sample rate for a given resolution). It must be noted, however, that the nominal resolution of ADCs is seldom achieved over the entire range of signal input frequencies. It is customary to use signal-to-noise (SNR) measurements (typically with single-tone sinusoidal inputs) to define effective bits versus input frequency. Measurements typically show that the number of effective bits falls off from the nominal value by at least 1.5 bits at the Nyquist frequency.

The problem of making high-performance ADCs is generally viewed as being considerably more difficult than for DACs. For ADCs, there are a variety of fundamental issues limiting performance. Input thermal noise voltage is one problem, which increases with increasing bandwidth and input impedance level. It is further exacerbated by noise contributions of transistors within the ADC. Another important problem is variation in the timing of the actual effective sampling instants from those of an ideal clock (aperture jitter). The jitter leads to errors that are increasingly severe for signals with higher slew rate. The aperture jitter for the state-of-the-art ADCs is of the order of 1 pS. Higher $f_t$ transistors may lead to decreases in this quantity. There are also inherent limits associated with the finite time for comparators to respond to input signals (termed regeneration time limit or comparator ambiguity limit). Fig. 3 shows representative limitations associated with these different factors.

A variety of ADC circuit approaches have evolved over decades of research. The flash architecture employs many comparators in parallel, leading to generally the highest speeds, although it has limited resolution because of the large transistor counts involved, as well as the difficulties of driving the large input capacitance and synchronizing the clocking of the comparators. An alternative high-speed approach derived from the flash is the folding amplifier approach, in which analog preprocessing allows reducing comparator number. In the pipeline and subranging architectures, several stages of conversion are done successively. Coarse quantization is done initially, followed by D/A conversion, and subtraction of the result from the incoming signal to produce a "residue" voltage corresponding to the portion of the signal not yet quantized. The residue is then amplified, and quantized in one or more following stages. The resolution of these approaches can be limited by errors in the DACs used or by the need to store signals during the initial conversion stages.

With high-speed technologies, the delta–sigma approach to A/D conversion has been growing in popularity. In this approach a low-resolution quantizer (often only a single comparator) is used to digitize the signal at a rate much faster than the Nyquist rate (providing oversampling ratios that may be above 200). The results of each quantization process are fed back and subtracted from the input. The residue is then filtered (with structures made up of a sequence of integrators or more complex circuits) and then passed to the quantizer. Fig. 4 shows a representative delta–sigma modulator loop. The delta–sigma technique allows spectrally shaping the quantization noise added by the A/D conversion process; it is removed to a large extent from the frequency band of interest. Subsequent to the delta–sigma

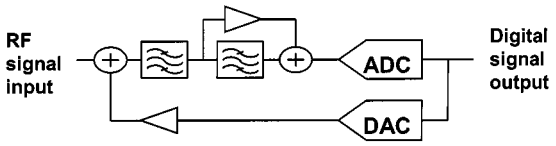


Fig. 4. Schematic architecture of a delta–sigma modulator.

modulator, the digital samples are filtered using DSP circuits to remove the out-of-band quantization noise so that decimation can be done.

For many approaches, it is worthwhile to employ a separate circuit to sample the input, and preserve its value during a portion of the digitization period. The characteristics of these sample-and-hold circuits may dominate the entire A/D converter performance regarding linearity, aperture time, and power dissipation.

Various high-speed technologies are better suited to one or another of these architectures and subcircuits. Bipolar technologies are preferred for flash converters, particularly because their excellent matching characteristics allows comparators with low offset voltage and high speed. Current sources for DACs are also realized most readily with bipolar devices. Analog switches, as required in sample-and-hold circuits, are most easily accomplished with FETs; bipolar ICs often resort to diode bridge switches to accomplish the S/H function. CMOS technology provides very good switches, and often employs switched capacitor approaches for the implementation of the circuits (for example, delta–sigma or pipeline converters). For these, the sample-and-hold function is intrinsic to each stage.

For microwave systems, a dominant push has been to digitize at the IF band, with SNR large enough to accommodate in-band interferers alongside weak signals. SNRs on an order of 85 dB are required; hence, 14-bit resolution has been a frequent target. Bandwidths on order of 10 MHz are now available, and bandwidths of 100 MHz are eagerly being pursued. A second-order low-pass delta–sigma modulator using continuous time integrators was demonstrated in an InP HBT IC technology in 1995 [24]. At a sample rate of 3.2 GHz and a signal bandwidth of 50 MHz $(\mathrm{OSR} = 32)$, the delta–sigma modulator demonstrated a spur-free dynamic range (SFDR) of 71 dB and at the ideal SNR of 55 dB for a second-order modulator operating at an oversampling ratio of 32. The modulator operated off of $\pm 5$-V supplies and dissipated 1 W of power.

The prospect of digitizing at RF has remained an attractive possibility for broad-band signals. Demonstrations have been made of digitizing at the level of 3–6 bits with sampling frequencies well into the microwave region. Fig. 5 presents a chip photograph of an integrated 6-bit 4-GS/s flash ADC, implemented with GaAs HBTs [25]. An InP HBT 3-bit flash ADC has been fabricated, which operates up to 18 GS/s, with 1.7 effective bits over the full Nyquist bandwidth. The 3-bit ADC has 960 transistors and dissipates 4.25 W of power [26].

## V. Digital Frequency Generation

Synthesis of sinusoidal signals of specified frequency is a central concern in most microwave systems. Frequency synthesizers are characterized by frequency range or bandwidth,

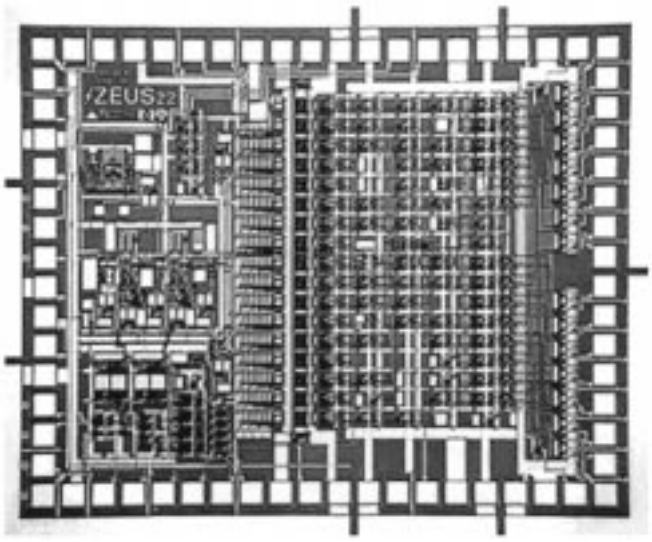


Fig. 5. Chip photograph of 6-bit 4 GS/s ADC fabricated with GaAs HBTs.

step size or frequency resolution, phase noise performance, switching speed, coherence of signals during switching, discrete spurious frequency outputs, as well as power dissipation and cost. Over the past decade, there has been an increasing use of digital techniques to address these issues [27]–[29].

Phase-locked loops are among the most common techniques to synthesize sinusoidal signals, as well as to recover clocks and other synchronization signals from data streams. Fig. 6 illustrates a representative phase-locked loop, containing a voltage-controlled oscillator (VCO), frequency divider, phase comparator, and phase filter. Digital (ring oscillators) or analog circuits may be used for the VCO, while the frequency dividers are almost universally implemented with digital techniques. As described in Section III, fixed modulus dividers operating up to 80 GHz have been demonstrated. Phase-locked loops synthesizing frequencies up to 40 GHz have been demonstrated with digital dividers; dynamic dividers can be used in this application, to achieve higher speed or save power. Variable modulus dividers permit easy frequency control; division by integer $N$ is most frequently used. For some communications applications the frequency resolution needed is finer than that provided by convenient reference frequencies (which, if too small, lead to unacceptable loop bandwidths and long settling times). For these situations, dividers with fractional divisors have been developed. In these, effectively, the frequency is divided alternately between $N$ and $N + 1$, where $N$ is an integer less than the desired divider ratio. The alternation of divisors tends to produce noise, but for a system designed with noise-shaping techniques, this noise can be largely removed from the frequency band of interest.

A potentially more powerful technique for signal synthesis is the direct digital frequency synthesis (DDS) approach, in which sinusoidal signals are built up by computing digital representations of $\sin(\theta(t))$, and then converting them to analog form with a DAC, as shown in Fig. 7. To generate the phase $\theta(t)$, a digital accumulator is used. To find $\sin(\theta)$, a lookup table is frequently employed, although a variety of approaches have been developed that can avoid the delay associated with ac-

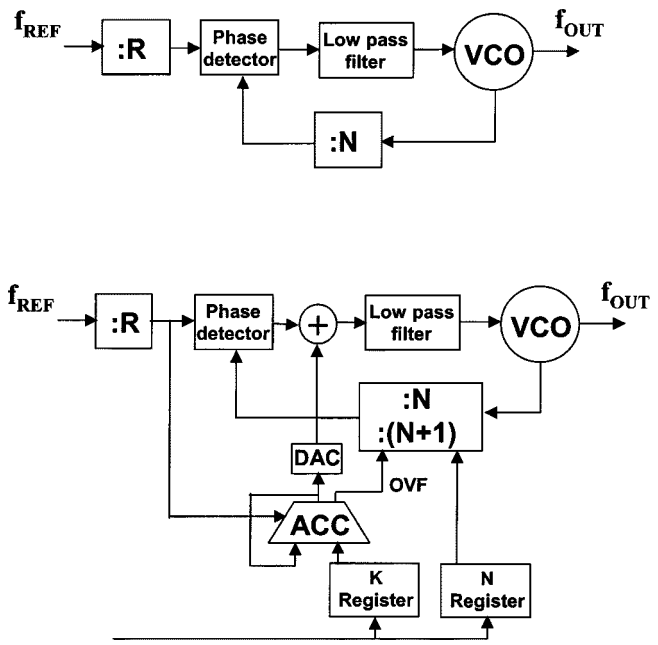


Fig. 6. Schematic architecture of a phase-locked loop with: (a) integer-$N$ and (b) fractional-$N$ digital dividers.

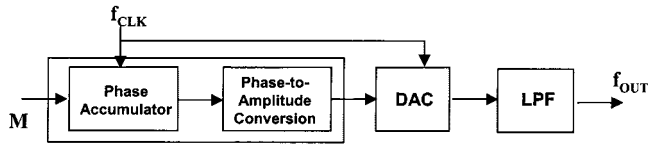


Fig. 7. Schematic architecture of a DDS.

cessing a large memory. The DDS approach has the advantages of very high-frequency resolution (in some cases, into the megahertz range), rapid switching between output frequencies, and the ability to change between frequencies while maintaining continuous phase. The DDS technique is the approach of choice for frequency-hopping spread-spectrum signal generation currently in use at modest frequencies (up to 10 MHz). The signal purity can be good, although a pacing element is the performance of the output DAC. At the high end, clock frequencies up to 2 GHz have been demonstrated, with a nominally 10-bit DAC resolution. The first monolithic GaAs DDS was reported in 1992. A 32-bit pipelined accumulator and a 10-bit DAC were used, integrated in a GaAs HBT-based IC. The maximum clock frequency reached 1 GHz. With nominal 500-MHz clocks, the worst-case spurious frequency in the output was below −55 dBc. Current research focuses on clock frequencies as high as 10 GHz.

The approach used in the frequency synthesizer can very easily be generalized to other waveforms, by simple processing of the output signal or changing the content of the lookup table. Phase modulation can be imposed on the DDS output with simple techniques. More generally, "arbitrary waveform generation" can be accomplished, which is particularly useful in instrumentation.

## VI. DSP

The inherent flexibility of DSP has led to a wide range of system applications. Many signal-processing functions are currently carried out at baseband frequencies, although they can be expected to move to larger bandwidths and IF frequencies in the future. In the following, a number of representative examples are described; however, the coverage is by no means exhaustive.

1) *Signal delay and storage*: Once digitized, signals can be readily delayed by almost arbitrary time intervals, or even stored for extended periods of time. This function is relatively difficult to accomplish in the analog domain. The storage and delay capability is used in instrumentation, and in RF memories (which have applications in electronic warfare). The capability is also central to the use of DSP techniques in active antenna arrays featuring true time delay. In these systems, the modulation and carrier frequency are delayed to a different extent among the elements of the array, to allow beam steering, adjustable nulling, etc. If the corresponding function is accomplished with (narrow-band) phase shifters, then there is an inherent loss of accuracy in the beam formation and unwanted sidelobes.
2) *FFT-based techniques*: Digital computations are a powerful technique to determine the spectral density of signals, or to generate signals with a specified spectral density. The technique is critical to radar signal processing. It is also exploited in wireless communications to generate signals that transmit information in adjacent frequency channels very closely spaced in frequency. This modulation approach, known as "orthogonal frequency division multiplexing," is emerging as a particularly important standard since the effects of wireless propagation time delay and fading can be tolerated within each one of the closely spaced channels individually, but not for an equivalent composite signal occupying the entire bandwidth.
3) *Nonlinearity compensation and predistortion*: In many microwave systems, particularly communication systems with spectrally efficient modulation formats, the transmitted signal must be linearly amplified. However, many power amplifiers, particularly when operated in the most efficient fashion, introduce nonlinearities. It is possible to apply predistortion to the signals to "undo" the amplifier nonlinearities [30], [31]. Digital predistortion offers a powerful technique for accomplishing this since any desired nonlinearity can be implemented. Also, the values used for predistortion can be altered as needed to correspond to changing amplifier characteristics, ambient temperature, etc., through "adaptive" techniques.
4) *Nonlinear signal generation*: In a variety of circumstances, it is necessary to generate signals that have a specified nonlinear relationship to input signals. The resultant computations are often hard to carry out with analog circuits. For example, in the linear amplification with nonlinear components (LINC) [32]), it is necessary to generate drive signals $s_1(t)$ and $s_2(t)$ for an amplifier pair that are derived from the input signal $s(t)$ using the relations

$$s_1(t) = s(t) + x_1(t)$$
$$s_2(t) = s(t) - x_1(t)$$

and

$$x_1(t) = ja(t)\sqrt{\frac{a_{\max}^2}{|a^2(t)| - 1}}. \tag{4}$$

The use of DSP allows computing the resulting signals in simple fashion, while it is difficult to do with analog electronics.

5) *Signal cancellation*: In a receiver, the elimination of signals corresponding to (intentional or unintentional) interferers is a central concern. In traditional microwave systems, the cancellation of these signals is done on the basis of the frequency spectrum alone (with the use of narrow filters at RF, IF, and baseband). With DSP techniques, the elimination of interferers can be done more flexibly. In CDMA, correlation or matched filtering, carried out with DSP, is used to separate the signal for a given user from those of others occupying the same frequency channel. In an extension of this approach, multiuser signal detection can be done (for example, at base-stations) in which the signals from all the users can be simultaneously analyzed.

## VII. Future Opportunities

The inexorable advancement of digital IC technology will provide many opportunities for the improvement of microwave systems. In many of these, the digital inputs and outputs will remain at baseband (below 10 MHz); in others, the DSP will be involved at IF, and in others, at RF.

The use of digital techniques at baseband is likely to become a pervasive feature of future systems. It is possible to envision "smart RF frontends" in which digital circuits not only generate the baseband signals, but also sense the condition of the RF front-end components (regarding temperature, supply voltage, power dissipation, overload condition, or even impedance matching or nonlinearity) and make adjustments to them through the use of variable bias conditions and power supply voltage, variable impedance matching, etc.

The use of DSP to generate communication signals though complex modulation is likely to progress toward ever-increasing bandwidths, both as a way of simplifying the following analog circuitry, and to accommodate the increasing bandwidths of signals needed for high data-rate communications.

DSP may be used in the future to generate signals that can be used directly at RF. This entails digital upconversion, as well as modulation. An interesting possibility is the use of DSP to generate the output RF signal as a single-bit-output data stream. This output can be fed to a switching-mode power amplifier (which acts as little more than a 1-bit power DAC), and a filter can be used to eliminate any resultant out-of-band noise (preferably recycling the associated power rather than absorbing it). A possible modulation format, which allows desirable communication signals with a time-varying envelope to be embedded in a single bit stream, is based on delta–sigma modulation [33]. In this approach, the entire transmitter is realized as a digital circuit, with the exception of a switching-mode amplifier and filter at the output, as shown in Fig. 8.

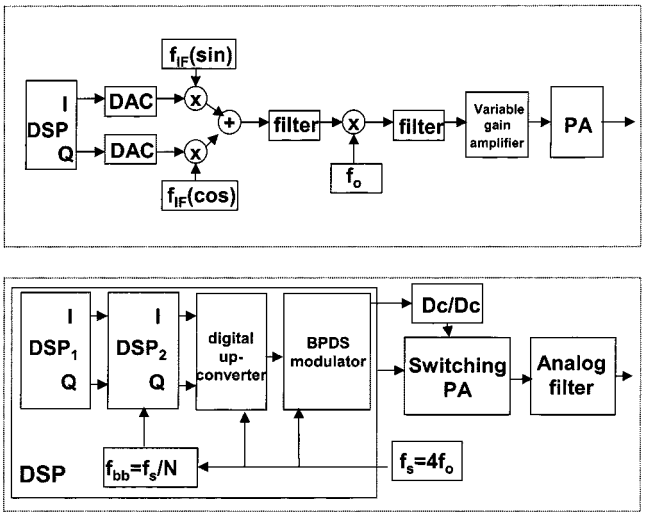


Fig. 8. Architecture of a conventional RF transmitter and, for comparison, that of a possible DSP-based RF transmitter.

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